REMARKS

Claims 1 to 3, 5, 7, 9, 13 and 16 to 18 have been amended of which allowable claims 5 and 13 have been rewritten in independent form. Claims 1 to 20 remain active in this application. Please charge any costs to Deposit Account No. 20-0068.

The objection to the disclosure is not understood and therefore respectfully traversed. It is respectfully submitted that all structure and method steps as claimed are fully set forth in the specification. There are no claims to a third order filter, only a first order and a second order which are shown as elements 24 and 26. It is also respectfully noted, that, though the theory of operation is stated, it is not necessary that an inventor know how or why the invention operates in the manner as stated. It is merely necessary that the invention be described in a manner that complies with 35 U.S.C. 112, first paragraph and this has been done since a full circuit is shown in Figs. 1 and 2.

Claims 1 to 4, 6 to 12 and 14 to 17 were rejected under 35 U.S.C. 103(a) as being unpatentable over Benabes et al. article (Passive sigma-delta converter design) in view of Chen et al. article (A 0.25 mW 13b passive $\Sigma\Delta$ modulator for a 10 MHz IF input) and Yamakido et al (U.S. 5,227,795) or Voorman et al. (U.S. 5,103,228). The rejection is respectfully traversed.

Claim 1 relates to a sigma-delta modulator using a passive filter which minimizes power consumption and improves speed relative to prior art which used active filters. The modulator includes, among other features, a passive discrete time circuit for receiving a digital feedback signal and an input signal, the input signal comprising information and one or more analog input currents, converting the digital feedback signal into an analog feedback signal during a first discrete time and summing the analog

feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals. No such structure or the combination as claimed is taught or suggested by any of the cited references taken either alone or in any proper combination. There is no teaching or suggestion in any of the references to combine them, even were they to teach that which is claimed, which they do not. In fact, the Chen et al. reference cited is authored by the applicant herein. Clearly, the combination as suggested by the examiner, even were it to be proper, was not apparent to the author of that reference at the time the reference was published. It follows that the rejection is based upon the misplaced clairvoyance of the examiner rather that a correct reading of the cited references.

Claim 1 further requires a passive continuous time circuit comprising a plurality of passive elements, the continuous time circuit coupled to the discrete time circuit to filter the one or more summed signals using a first-order filter and a second-order filter ~~in order~~ to generate one or more filtered signals, the first-order filter comprising one or more first passive elements of the plurality of passive elements, the second-order filter comprising one or more second passive elements of the plurality of passive elements. No such structure or the combination as claimed is taught or suggested by any of the cited references taken either alone or in any proper combination. There is no teaching or suggestion in any of the references to combine them, even were they to teach that which is claimed, which they do not. In fact, the Chen et al. reference cited is authored by the applicant herein. Clearly, as stated above, the combination as suggested by the examiner, even were it to be proper, was not apparent to the author of that reference at the time the reference was published. It follows that the rejection is based

upon the misplaced clairvoyance of the examiner rather that a correct reading of the cited references.

Claims 2 to 4 and 6 to 8 depend from claim 1 and therefore define patentably over the applied references for at least the reasons set forth above with reference to claim 1.

In addition, claim 2 further limits claim 1 by requiring a transconductance circuit to receive the input signal comprising the information, the input signal having one or more analog input voltages and convert the one or more analog input voltages into one or more analog input currents. No such combination is taught or suggested by the applied references taken alone or in any proper combination.

Claim 3 further limits claim 1 by requiring that the discrete time circuit convert the digital feedback signal into an analog feedback signal using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time. No such feature is taught or suggested by the applied references taken alone or in any proper combination either a lone or in the combination as claimed.

Claim 4 further limits claim 1 by requiring that the one or more first passive elements associated with the first order filter comprise a first capacitor and the one or more second passive elements associated with the second order filter comprise a second capacitor and a resistor. No such combination is taught or suggested by the applied references taken alone or in any proper combination.

Claim 6 further limits claim 1 by requiring that the one or more second passive elements associated with the second order filter comprise a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated

with a resistance and the second capacitance and the resistance selected according to a frequency response corresponding to a direct current frequency. No such structure is taught or suggested by the applied references taken alone or in any proper combination either alone or in the combination as claimed.

Claim 7 further limits claim 1 by requiring that the quantizer comprise a comparator to generate the digital signal using the one or more filtered signals byamplifying the one or more filtered signals and comparing the one or more filtered signals to each other to quantize an error associated with the input signal and the digital signal. No such structure is taught or suggested by the applied references taken alone or in any proper combination either alone or in the combination as claimed.

Claim 8 further limits claim 1 by requiring that the output of the quantizer be coupled to the discrete time circuit in order to form a passive feedback loop, the passive feedback loop operable to convert the digital signal into an analog feedback signal. No such structure is taught or suggested by the applied references taken alone or in any proper combination either alone or in the combination as claimed.

Claim 9 relates to a method for converting an input signal into a digital signal, and requires, among other steps, receiving a digital feedback signal and an input signal at a discrete time circuit, the input signal comprising information and one or more analog input currents, converting the digital feedback signal into an analog feedback signal during a first discrete time. summing the analog feedback signal and the one or more analog input currents during a second discrete time to yield one or more summed signals and filtering the one or more summed signals at a continuous time circuit in order to generate one or more filtered signals, the continuous time circuit comprising a passive

first-order filter and a passive second-order filter, the first-order filter comprising one or more first passive elements of the plurality of passive elements, the second-order filter comprising one or more second passive elements of the plurality of passive elements. No such steps are taught or suggested by the applied references taken alone or in any proper combination in the above combination or in the total combination as claimed.

Claims 10 to 12 depend from claim 9 and therefore define patentably over the applied references for at least the reasons stated above with reference to claim 9.

In addition, claim 10 further limits claim 9 by requiring receiving at a transconductance circuit the input signal comprising the information, the input signal having one or more analog input voltages and converting the one or more analog input voltages into the one or more analog input currents. No such combination is taught or suggested by the applied references taken alone or in any proper combination taken alone or in any proper combination.

Claim 11 further limits claim 9 by requiring that converting the digital feedback signal into an analog feedback signal during the first discrete time further comprise using a reference voltage, the reference voltage supplied by a reference capacitor, the reference capacitor charged to the reference voltage during the first discrete time. No such combination is taught or suggested by the applied references taken alone or in any proper combination taken alone or in any proper combination.

Claim 12 further limits claim 9 by requiring that the one or more first passive elements associated with the first order filter comprise a first capacitor and the one or more second passive elements associated with the second order filter comprise a second capacitor and a resistor. No such combination is taught or suggested by the applied

references taken alone or in any proper combination taken alone or in any proper combination.

Claim 14 further limits claim 9 b y requiring that the one or more second passive elements associated with the second order filter comprise a second capacitor and a resistor, the second capacitor associated with a second capacitance, the resistor associated with a resistance and the second capacitance and the resistance selected according to a frequency response, the frequency response corresponding to a direct current frequency. No such combination is taught or suggested by the applied references taken alone or in any proper combination taken alone or in any proper combination.

Claim 15 further limits claim 9 by requiring that generating the digital signal using the one or more filtered signals further include amplifying the one or more filtered signals and comparing at a comparator the one or more filtered signals to each other to quantize an error associated with the input signal and the digital signal. No such step is taught or suggested by the applied references taken alone or in any proper combination taken alone or in any the combination as claimed.

Claim 16 further limits claim 9 by requiring that the output of the quantizer be coupled to the discrete time circuit to form a passive feedback loop, the passive feedback loop converting the digital signal into an analog feedback signal. No such combination is taught or suggested by the applied references taken alone or in any proper combination taken alone or in the combination as claimed.

Claim 17 requires, among other features, means for filtering the one or more summed signals at a continuous time circuit in o rder to generate one or more filtered signals, the continuous time circuit comprising a passive first-order filter and a passive

second-order filter, the first-order filter comprising one or more first passive elements of the plurality of passive elements, the second-order filter comprising one or more second passive elements of the plurality of passive elements. No such combination is taught or suggested by the applied references taken alone or in any proper combination taken alone or in the combination as claimed.

With reference to claim 18, no objection thereto has been found in the Office action as stated. Accordingly, should there be an objection to claim 18, it is respectfully requested that the objection be stated so that appropriate action can be taken in regard thereto.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,

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